A single-stage, two-channel Ka-band to digital, thermal compensating receiver for SWOT

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Abstract: **In this paper, we discuss the progress being made on the design and construction of the single-stage, two-channel Ka-band thermal compensating receiver for the Surface Water and Ocean Topography mission (SWOT). The fundamental signature utilized by SWOT for performing topographic measurements of the ocean and surface water is that of the interferometric phase between two channels in the receiver. While the frequency of 35 GHz has the advantage of a compact spacecraft structure and allowing a high spatial resolution at a low proportional bandwidth (200 MHz BW), challenges exist in the receiver at keeping the two interferometric channels isolated from one another while also requiring a thermal symmetry in order to minimize temperature gradients in the receiver system which will effect the interchannel phase. In this paper, we present a preliminary design for a single-stage downconversion from Ka-band to L-band (1.2 GHz) and the subsequent direct sampling controlled by two 3 GSamp/sec ADC's and an FPGA which performs digital downconversion and thermal compensation.**

I. Introduction

The performance of radar interferometry at millimeterwave frequencies, such as Ka-band (35 GHz; 8.5 mm) can be particularly useful for the study of wide-swath topographic mapping of earth-science targets that decorrelate quickly over time. In the case of the Surface Water and Ocean Topography (SWOT) mission, one of the NRC's second tier decadal survey missions is such an interferometer, whose water-based target of interest changes its electromagnetic signature at time sclaes on the order of milliseconds to seconds. While altimetric methods for measuring topography exist for ocean and land-based water targets, these measurements tend to be narrow-swath, and hence difficult to generate mid- to large-scale models for the target dynamics over both short and extended periods of time. For this reason, a wide-swath mapping instrument (such as SWOT) utilizes near-nadir fan-beam to perform radar interferometry which results in high-resolution and wide swath measures of topography. Because the sensitivity of radar interferometry to topographic height is governed by the ratio of interferometric baseline to frequency, single-pass interferometric instruments are more compact (and able to fly on a single platform) compared to their lower frequency counterparts (e.g. L- or C-band interferometers), thus eliminating the error source associated with temporal decorrelation or the high cost of flying two satellite platforms simultaneously. With the advantage of flying a compact instrument on a single platform, comes an increased sensitivity of the interferometric phase to the mechanical and thermal aspects that govern the interferometer's observational geometry.

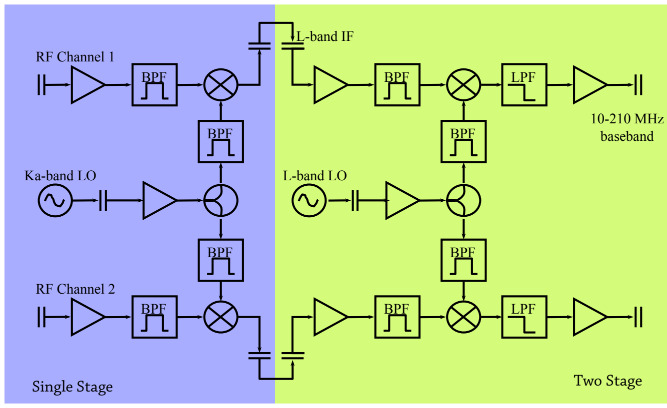

Figure 1. *A simplified version of the digital-side of the interferometric downconverter. Analog science data is ingested at left by two high-speed A/D converters, demultiplexed and read into the FPGA. Thermal and functional telemetry received from the RF downconverter is blended within the FPGA for choosing the optimal filter specifications for further processing.*

One component of the interferometric design that is important in the overall system performance, is that of the interferometric, two-channel downcoverter, which converts the high-frequency signal to a lower frequency, suitable for digital sampling and further processing. The reason that the downconversion can be particularly sensitive, is that the science data must undergo one (or more) levels of non-linear operation using analog devices that are in close-proximity to one another. Hence, the potential exists for significant crosstal between the supposedly independent observations made by the interferometric system, as well as for an imbalance in the way that one channel may be processed with respect to the other.

For this reason, the University of Massachusetts and NASA's Jet Propulsion Laboratory have been cooperating on the development of a Ka-band interometric downconverter, that can both monitor the electro-thermo effects on the downconversion process, and make corrections in the digital subsystem for imbalances that may occur to the two interferometric channels. Further, to improve isolation between the downconversion channels, and to facilitate the use of thermally dependent digital filters, we have been investigating the tradeoffs associated with digital sampling at a high intermediate frequency (3 GSamp/sec) versus a lower frequency (500 MSamp/sec), to achieve a wide bandwidth (200 MHz) of digital science data suitable for interferometric processing.

Shown in Figure 1 above, is an RF block diagram that highlights the two methods for downversion, one being single-stage, and the other two-stage, and how they can be leveraged to find the most advantageous approach for downconverting interferometric data.

The output of the single- or two-stage downconverted analog signal is then fed into a digital subsystem that is also capable of receiving thermal and electrical-status (power, current and voltage) telemetry from the analog portion of the downconversion process (Figure 2). Thus, the two interferometric data streams can be blended with the telemetry data, to characterize and ultimately compensate for thermally and electrically sensitive components of the analog downconversion process.

In this short paper, we review the progress that has been made to date on the single-stage dowonconverter part of this project's work, as well as the development of the digital board that will be capable of ingesting two channels of 3 GSamp/sec interferometric data, telemetry data, and capapble of filtering and processing to create two, thermally compensated streams of digital data with a 200 MHz (or better) bandwidth, suitable to serve as the prototype downconverter for the SWOT mission.

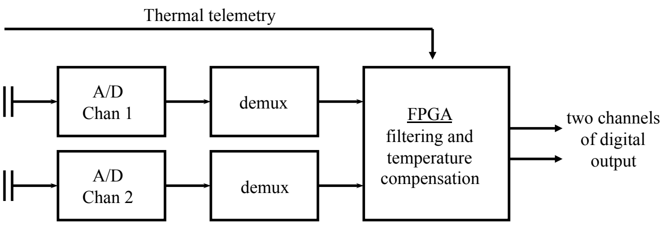

Figure 2. *A simplified version of the digital-side of the interferometric downconverter. Analog science data is ingested at left by two high-speed A/D converters, demultiplexed and read into the FPGA. Thermal and functional telemetry received from the RF downconverter is blended within the FPGA for choosing the optimal filter specifications for further processing.*

II. DIGITAL DEVELOPMENT

The digital side of the development, while complex, has been straight-forward, consisting primarily of two National Semiconductor ADC08D1520 Analog to eight-bit Digital Converter (ADC) chips configured to sample at 3 GSamp/sec (Figure 3) a high capacityXilinx Data processing FPGA, and a lower capacity Xilinx communications FPGA, suitable for interfacing with the PCI bus. The Data processing FPGA is capable of filtering and downsampling the high-data rate streams to a lower data rate and lower bandwidth as well as interfacing with components over standard JTAG, SATA and SFP interfaces. Coefficients for the filters used for the data downconversion and subsampling are stored in lookup tables on-board the ADC's and are available for application based on the status of the telemetry being read in from the analog portion of the downconverter.
While the final digital board has not been completed as of this writing, the placement and routing for the board with a 6U standard size has been, as shown in Figure 4. In this figure, the major components are identified, where the two ADC's are identified at left, along with a 24-pin header, which carries the telemetry and trigger signals. The digital board itself has been fundamentally designed with simplicity and spaceborne component compatability in mind, thus allowing it to serve as a direct prototype for what ultimately may end up as the ADC/ digital subsystem for the SWOT mission.

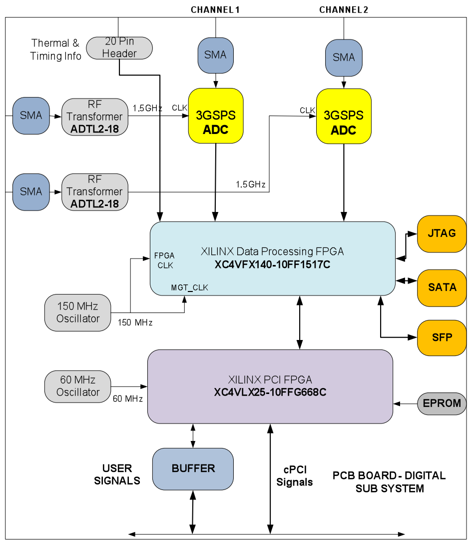

Figure 3. *Block diagram of the Analog to Digital Converter subsystem interfaced to a data processing FPGA. Signals are read in at 3 GSamp/sec and output through a communications FPGA that interfaces to the PCI bus.*

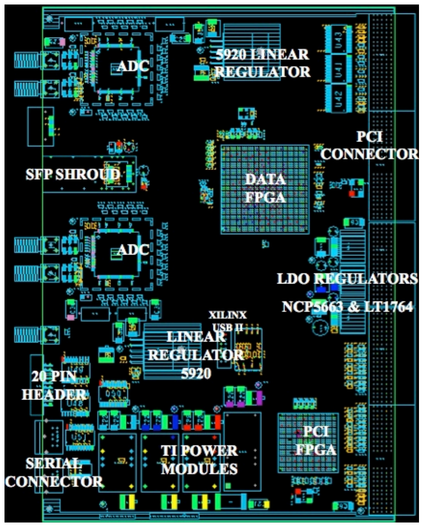

Figure 4. *The physical layout of the digital subsystem, as it fits on a 6U geometry board. RF and low-frequency telemetry signals are sampled at left, processed by the data FPGA, and expressed on the PCI bus through a separate FPGA.*

III. RF DEVELOPMENT

A. *Design*

The RF portion of this work is strongly influenced by previous work done by our team on a similar Ka-band, 20 MHz BW, development (Figure 5; see also [1,2, & 3]). In short, a 34.55 GHz LO is fed in to the downconverter, amplified, and then split into two channels by a rat-race power divider which has been tuned to minimize reflections. The split LO power is fed through one of two shielded two microstrip filters, one for each side of the downconverter, which have been design to pass the LO frequency, but to reject RF signals from either side of the downconverter; hence providing a barrier to signals that may inadvertently communicate with one another through the common LO path.

Two hundred MHz bandwidth science data at 35.75 entering on one of the two interferometric channels, is first amplified and filtered (for image and LO rejection) prior to mixing to L-band. Additional components on the L-band board consist of low-frequency A/D converters and sensors capable of delivering temperature, power, and current, telemetry through a 24-pin ribbon cable that also provides power to the board. In addition to isolation cavities that cover the regions of the board with microstrip filters, one-quarter inch wide via strips additionally separate the two interferometric channels (top and bottom) from the common LO distribution and power conditioning portion of the Ka-band downconverter board (middle section of Figure 5). Walls from the mechanical housing are designed to mate with these via-strips using a compressible conductive “sock”, which forms a sufficient electric connection with the ground plane and to improve electromagnetic isolation between critical regions of the downconverter’s architecture.

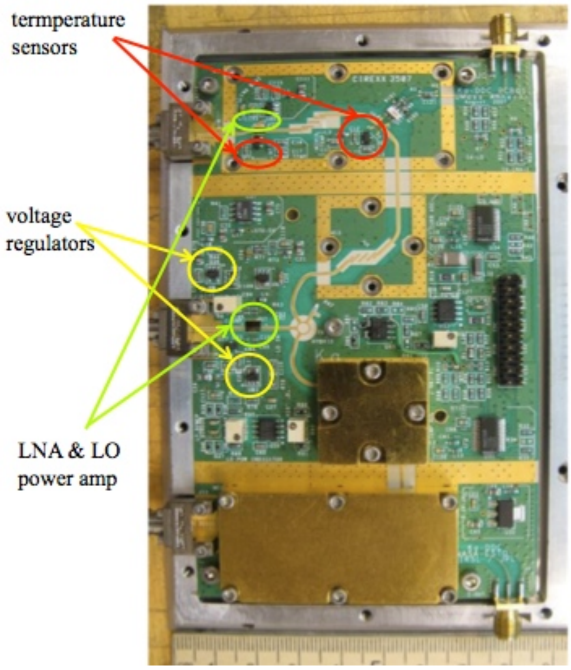

Figure 5. *The single-stage Ka-band downconveter board. Shown at bottom is a wooden ruler showing 1/2cm major units. Shown on the board are the locations of some of the temperature sensors, as well as regions where the majority of thermal heat is generated on the board. The lower half of the board is seen to be populated with two isolation cavities (golden boxes) which are placed over the microstrip filters, similar to those seen in the upper half of the circuit.*

B. *Thermal Analysis*

Among the high-priority development paths for this project has been to improve the thermal analysis of the components (amplifiers, mixers, filters, etc.) and transmission lines for the high-frequency portion of the board. To this end, a power analysis for the active parts has been coupled with a two-dimensional thermal model (from COMSOL) that takes into account the highly heat-conductive outer walls of the downconverter chassis (Figure 6). The thermal model, coupled with temperature measurements at point locations on the board, has led to a modeling accuracy better than 5% agreement, which can then be used to understand the sources of thermally dependent phase imbalance between the two channels of the interferometric downconverter.

One example of the differential phase that can be induced in the downconverter is shown in Figure 7, where the phase difference between the two interferometric channels is measured over time. To measure the phase difference to a high degree of accuracy (better than 3 millidegrees), a maximum likelihood technique was developed [3]. The figure also shows a best fit, second order polynomial which has been correlated with the physical temperature of the downconverter, which was allowed to stabilize to 45 degrees C in a thermally isolated environment over a five hour period of time. Worthy of note in the figure is that the interferometric phase changes over time, by approximately 0.5 degrees, much larger than the system specification for SWOT. A better understanding of the source of the thermally induced phase imbalance will lead to a better design for the downconverter, and the ability to compensate for thermal effects in the data stream.

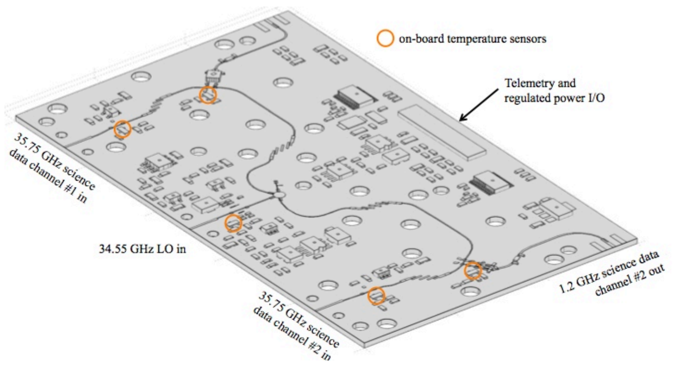

Figure 6. *A mechanical layout of the two-dimensional thermal analysis that is conducted for the interferometric downconverter. Shown on the board are the parts placement and the location of temperature sensors on the board, used to provide thermal measurements and check the accuracy of the model.*

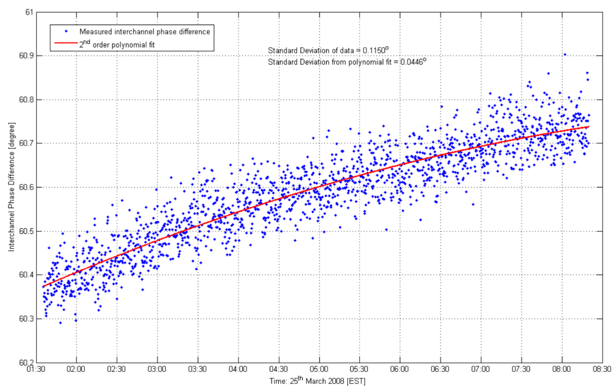

Figure 7. *Differential phase measured as a function of time over a seven hour period. Shown in the diagram are individual phase measurements made very 30 seconds, and a best fit second order polynomial to the phase. It has been shown that the shown trend in phase difference is associated with a slow temperature change in the downconverter due to active components heating the chassis over time.*

An example of the thermal analysis that was performed on the downconversion board is shown in Figure 8. In the one part of the figure (right side), a two-dimensional thermal analysis is performed using the COMSOL software program which calculates the temperature distribution within the downconverter board, based on a constant temperature for the mechanical housing and thermal inputs being deposited on the board by various active components; dominant among them, the two low-noise amplifiers for the science data, and the main amplifier for the local oscillator input.

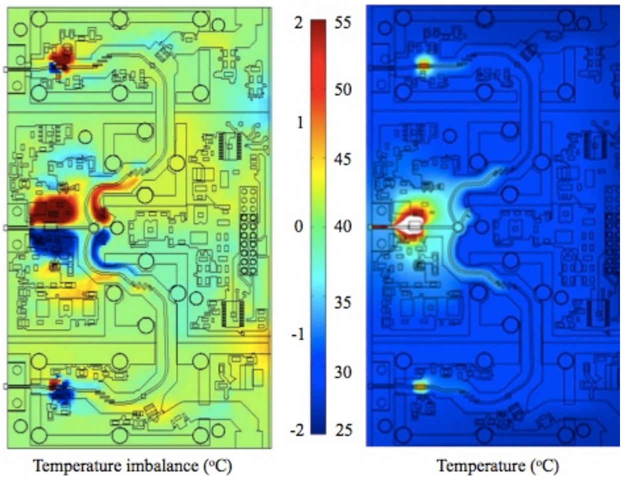

Figure 8. *Thermal analysis of the Ka-band single-stage downconverter board performed by the COMSOL software. Shown at left is the thermal imbalance between the upper and lower parts of the board, while at right, is the temperature of the downconverter board calculated from the power being dissipated by the active components on the board. Dominant among the components contributing to the heat of the board, are the two signal LNA's and the LO power amplifier.*

With the given thermal analysis shown on the right side of Figure 8, it is also possible to explore the temperature imbalance between the upper and lower parts of the board, which are essentially symmetric. The clear thermal imbalance shown in the image, on the order of two degrees, results from slight asymmetries in the placement of the active components, and in the layout of thermally conductive components on the downconverter. While it remains to be determined to what degree these thermal imbalances effect the electrical path length for the science data on the two interferometric channels, the method for doing so will rely on the relationship between the physical temperature of the board and the thermal expansion coefficient of the board materials. The treatment shown at left will lend itself to performing this next step in the analysis and for better understanding the sensitivity of interferometric phase to temperature, as shown in Figure 7.

The next stage of thermal analysis development will look more closely at the dynamics of thermal change, both in terms of measurement and modeling, and then correlating the thermal changes, both from point measurements and distributed across the downconverter, to observations of phase difference changes between the interferometric channels. This analysis will then provide thermal stability requirements that may be levied on the spacecraft, as well as to compensate for the thermal effects in the digital side of the processing chain. Lastly, the thermal analysis described so far, will also help to better design the next version of the downconverter, anticipated to be implemented by our group in the near future.

IV. Conclusions

In this short paper, a single-stage two-channel interferometric downconverter was presented that included both the digital and analog subsystems. The digital subsystem will be capable of sampling two L-band data streams at 3 GSamp/sec, and compensating for temperature effects on the analog downconversion via measurements made by thermal, and electrical telemetry measured on-board the downconverter. The downconverter itself is being thermally modeled to better understand the distribution of temperature on the downconverter and to inform the design for achieving better stability as a function of a changing thermal environment.

Acknowledgment

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